REMARKS

In the Office Action mailed on January 7, 2005, claims 1-4 are rejected under 35 USC §112, second paragraph, as being indefinite. Claim 32 is objected to in view of a typographical error. Claims 1-2, 4-7, 21-24 and 32 are rejected under 35 USC §102(b) as being anticipated by Seefeldt et al. (U.S. Patent 4,978,633, "Seefeldt"). Claim 3 is rejected under 35 USC §103(a) as being unpatentable over Seefeldt in view of Cory et al. (U.S. Patent 6,617,877, "Cory"). Claims 25-29 are rejected under 35 USC §103(a) as being unpatentable over Seefeldt. Finally, claims 30 and 31 are allowed.

In response to the objection to claims 1-4, Applicant has amended the claim to eliminate the term "column-like," and indicate that predetermined regions in an area are in a column. In response to the rejection of claim 3 under 35 USC §103(a) as being unpatentable over Seefeldt in view of Cory, Applicant respectfully submits that the rejection of the claims under 35 USC §103(a) is improper because Cory is only available as a reference under 35 USC §102(e). Because U.S. Patent 6,617,877 to Cory et al. and U.S. Application Serial No. 10/618,404, at the time the invention of U.S. Application Serial No. 10/618,404 was made, were both owned by Xilinx, Inc., Cory is removed as prior art under 35 USC §103(c) for the purposes of the rejection under 35 USC §103(a).

Response to Rejection of Claims under 35 USC §102(b) over Seefeldt

In response to the rejection of claims 1-2, 4-7, 21-24 and 32 under 35 USC §102(b) as being anticipated by Seefeldt, Applicant has amended each of the independent claims 1, 5, 21, 26 and 32 to distinguish over the reference. Seefeldt is directed to a gate array configuration that provides a variable size cell capacity. A matrix of intermingled gate supercells and input/output cells are selectively interconnected with one another by a set of global routing channels. (Col. 2, lines 3-9). Fig. 5 shows how the input/output supercells and gate supercells are repeated in the vertical and horizontal directions across a wafer. By intermingling the input/output supercells and the gate supercells as shown in Fig. 5, the size and the geometry of

the gate array is not fixed. For example, if a circuit design requires the use of twenty gate supercells and sixteen input/output supercells, the wafer is scribed along vertical scribe lines 251 and horizontal scribe lines 261 to obtain a 6X6 supercell. The smallest practical pattern of gate supercells and input/output supercells could formed by a 3X3 pattern of five gate cells and four input/output supercells at the corners. (Col. 5, lines 34-65). Accordingly, Seefeldt teaches away from the Applicant's claims by only teaching intermingling of input/output and gate logic cells, rather than columns as claimed by Applicant.

Referring to each of the independent claims individually, Applicant has amended independent claim 1 to indicate that:

> (i) predetermined regions in an area are in a column and substantially fill the area;
>
> (ii) wherein each of the predetermined regions in a first area comprises programmable circuits which are substantially identical and have a first function; and
>
> (iii) wherein each of the predetermined regions in a second area comprises programmable circuits which are substantially identical and have a second function.

Applicant respectfully submits that Seefeldt fails to disclose or suggest such areas which extend from one edge of an IC to an opposing edge, and have programmable circuits which are substantially identical as claimed. Applicant has further dependent claims 2-4 to conform to the amended claim 1. Accordingly, Applicant respectfully requests reconsideration of independent claim 1 as amended and dependent claims 2-4 in view of the amendments.

In response to the rejection of independent claim 5, Applicant has amended claim 5 to indicate that each region of a first column of the third set consists essentially of regions from the first set. Applicant submits that Seefeldt fails to disclose or suggest the regions and columns as claimed by Applicant, and respectfully submits that claim 5 as amended and dependent claims 6 and 7 are allowable over Seefeldt.

In response to the rejection of independent claim 21, Applicant has amended claim 21 to include a step of "providing a plurality of Input/Output blocks in a second

column, the second column extending from the first side of the integrated circuit to the second side of the integrated circuit." Applicant submits that Seefeldt fails to disclose or suggest a column of Input/Output blocks extending from the first side of the integrated circuit to the second side of the integrated circuit as claimed. Applicant respectfully submits that claim 21 as amended is allowable over Seefeldt. Applicant has also amended dependent claim 23 to more clearly claim the method of providing configurable logic clocks and Input/Output blocks. In particular, Applicant has amended claim 23 to correctly depend from claim 21 and indicate that "there is no input/output block disposed between the column of configurable logic blocks and the first side of the integrated circuit die." Finally, Applicant has further dependent claims 22, 24 and 25 to conform to the amended claim 21. Applicants respectfully submit that dependent claims 22-25 are also allowable over Seefeldt.

In response to the rejection of independent claim 26, Applicant has amended claim 26 to distinguish over Seefeldt. In particular, Applicant has amended claim 26 to include "a column of input/output block tiles," rather than a column including input/output block tiles. Applicant submits that Seefeldt fails to disclose or suggest a column of input/output block tiles as claimed by Applicant, and respectfully submits that claim 26 as amended and dependent claims 27-29 are allowable over Seefeldt.

Finally, in response to the rejection of independent claim 32, Applicant has amended claim 32 to indicate that the input/output block tile is "in a column of input/output block tiles extending from a first end to a second end." Applicant submits that Seefeldt fails to disclose or suggest a column of input/output block tiles extending from a first end to a second end as claimed by Applicant, and respectfully submits that claim 32 as amended is allowable over Seefeldt.

Response to Rejection of Claims under 35 USC §103(a) over Seefeldt

In response to the rejection of claims 25-29 under 35 USC §103(a) as being unpatentable over Seefeldt, Applicant respectfully submits that the claims are allowable in view of the amendments described above. In particular, Applicant submits that claim 25 is allowable for the same reason that independent claim 21 as amended is believed allowable. Applicant further submits that independent claim 26,

and its dependent claims 27-2, are allowable in view of the amendments to claim 26 as set forth above.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the Applicant's attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on April 5, 2005.

Pat Slaback
Name

Signature